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TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. YOR919980324US2

In Re Application Of: **Stephen M. Gates et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/080,568	February 25, 2002	Phat X. Cao	21254	2814	9141

Invention: **FORMATION OF ARRAYS OF MICROELECTRONICS ELEMENTS**

COMMISSIONER FOR PATENTS:

Transmitted herewith ~~is triplicate~~ is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **March 15, 2005**

The fee for filing this Appeal Brief is: **$500.00**

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Dated: 5/16/05

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May 16, 2005

VIA FACSIMILE
EXPEDITED PROCEDURE

To: Examiner Phat Cao
Group Art Unit No. 2814
U. S. P. T. O.

Facsimile No. 703-872-9306

From: Phillip E. Miller

Facsimile No. 703-761-2375

Re: Filing of Appellant's Brief on Appeal
U. S. Patent Application Serial No. 10/080,568
Our Ref: YOR.324DIV

Dear Examiner:

Enclosed please find Appellant's Brief on Appeal in the above-referenced patent Application.

Thank you in advance for your kind consideration of this case.

Very truly yours,

Phillip E. Miller

PEM/lnb
Enclosure

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10/080,568
YOR919980324US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Stephen M. Gates, et al.

Serial No.: 10/080,568 **Group Art Unit:** 2814

Filed: February 25, 2002 **Examiner:** Phat X. Cao

For: FORMATION OF ARRAYS OF MICROELECTRONICS ELEMENTS

Honorable Commissioner of Patents
Alexandria, VA 22313-1450

APPELLANT'S BRIEF ON APPEAL

Sir:

Appellant respectfully appeals the final rejection of claims 11-18, 26-31, 33-35 and 37-43 in the Office Action dated November 16, 2004. A Notice of Appeal was filed herein on December 15, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, assignee of 100% interest of the above-referenced patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant, Appellant's legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 11-18, 26-31, 33-35 and 37-43 are all the claims presently pending in the application and are set forth fully in the attached Appendix.

Claims 11-12, 18, 26, 28, 33, 38-41 and 43 stand rejected under 35 U.S.C. § 102(e) being allegedly anticipated by Lee et al. (U.S. Patent No. 5,895,947). Claims 11-12, 15-16,

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18, 26, 28-29, 33-35 and 37-38 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Durlam, et al. (U.S. Patent No. 5,940,319) and Lee. Claims 13-14, 17, 27 and 30-31 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Durlam and Lee and further in view of Bronner et al. (U. S. Patent No. 6,242,770).

Appellant respectfully appeals these rejections.

IV STATEMENT OF AFTER-FINAL AMENDMENTS

Appellant notes that an Amendment which canceled claim 36 and incorporated the subject matter of claim 36 **verbatim** into independent claims 11, 26 and 38 was filed on February 28, 2005. However, in an Advisory Action dated March 17, 2005, the Examiner stated that he refused to enter the Amendment because the proposed amendments "raise new issues that would require further consideration and/or search".

Appellant respectfully submits that the Amendment filed herein on February 28, 2005 clearly does not "raise new issues" as alleged by the Examiner. Therefore, on May 13, 2005, Appellant filed a Second After-Final Amendment which was substantially the same as the February 28th Amendment, to request that the Examiner reconsider his unreasonable refusal of entering the February 28th Amendment.

Appellant notes that the pending claims are included in the Appendix attached hereto, presuming entry of the February 28, 2005 Amendment.

V. SUMMARY OF THE INVENTION

The claimed invention (e.g., as recited in **independent claim 11**), is directed to an array of microelectronic elements including a substrate of semiconductor material, a lower layer of dielectric material disposed with a lower surface in contact with the substrate and an upper surface in spaced adjacency thereto, a pattern of mutually electrically isolated conducting regions disposed within the lower layer of dielectric material, the conducting regions extending to the upper surface of the lower layer, an upper layer of dielectric material disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer, a plurality of nodes of semiconductor material disposed within the upper layer of dielectric material, each of the nodes being in electrical contact with only one of the

conducting regions at the upper surface of the lower layer, and a bonding promoting layer formed on the lower layer of dielectric material, the bonding promoting layer bonding the lower surface of the upper layer of dielectric material to the upper surface of the lower layer (e.g., see Application at Figure 5B; and page 13, lines 9-12). Further, each conducting region includes a metal conductor, and a via which is filled with a diffusion barrier material, the diffusion barrier material extending between the metal conductor and a node in the plurality of nodes and electrically connecting the metal conductor with the node.

Another aspect of the claimed invention (e.g., as recited in **independent claim 26**) is directed to a microelectronic element array including a semiconductor substrate, a first dielectric layer formed on the substrate, a plurality of electrically isolated conductive regions disposed within the first dielectric layer. Each conductive region a metal conductor, and a conductive via which is filled with a diffusion barrier material formed on the metal conductor, a second dielectric layer having a lower surface which is bonded to an upper surface of the first dielectric layer, a plurality of semiconductor nodes formed in the second dielectric layer, each semiconductor node contacting the conductive via and being electrically connected to the metal conductor by the conductive via, and a bonding promoting layer formed on the first dielectric layer, the bonding promoting layer bonding the lower surface of the second dielectric layer to the upper surface of the first dielectric layer(e.g., see Application at Figure 5B; and page 13, lines 9-12). Further, the diffusion barrier material extends between the metal conductor and a node in the plurality of nodes.

Another aspect of the claimed invention (e.g., as recited in **independent claim 38**) is directed to a microelectronic element array including a first dielectric layer formed on a substrate, at least one electrically isolated conductive region formed in the first dielectric layer. The at least one conductive region includes a metal conductor, and a conductive via which is filled with a diffusion barrier material formed on the metal conductor, a second dielectric layer which is bonded to the first dielectric layer, and at least one semiconductor node formed in the second dielectric layer, the at least one semiconductor node being formed on and contacting the at least one conductive region, and a bonding promoting layer formed on the first dielectric layer, the bonding promoting layer bonding a lower surface of the second dielectric layer to an upper surface of the first dielectric layer(e.g., see Application

at Figure 5B; and page 13, lines 9-12). The diffusion barrier material extends between the metal conductor and the at least one semiconductor node and electrically connects the metal conductor to the at least one semiconductor node.

Conventional devices typically form a semiconductor node (e.g., a silicon diode) directly on an aluminum or copper metal conductor (e.g., a word line) (e.g., as illustrated in Figure 17 of the Durlam reference). However, such devices suffer severe problems. Namely, the metal conductor reacts with the semiconductor node, thereby making the devices unreliable.

To address this problem, it has been considered to the metal conductor (e.g., word line) may be made from a refractory metal. However, such refractory metal word lines have a high resistance, such that only small arrays of memory elements could be made (Application at page 8, lines 10-13).

The claimed invention, on the other hand, forms, in a lower dielectric layer, a via on a metal conductor which is filled with a diffusion barrier material, and forms, in an upper dielectric layer, a plurality of nodes (e.g., Application at Figure 5B). Further, a bonding promoting layer is formed on the lower dielectric layer, the bonding promoting layer bonding the upper dielectric layer to the lower dielectric layer (Application at 13, lines 9-12). The bonding promoting layer may help to promote bonding between the first dielectric layer and the second dielectric layer, when the inventive array is formed using a bonding process such as the SmartCutR process (Application at page 11, lines 1-18).

VI. GROUNDS OF REJECTION TO BE REVIEWED

The grounds of rejection to be reviewed by the Board of Patent Appeals and Interferences include:

1) rejection of claims 11-12, 18, 26, 28, 33, 38-41 and 43 under 35 U.S.C. § 102(e) being allegedly anticipated by Lee et al. (U.S. Patent No. 5,895,947);

2) rejection of claims 11-12, 15-16, 18, 26, 28-29, 33-35 and 37-38 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Durlam, et al. (U.S. Patent No. 5,940,319) and Lee; and

3) rejection of claims 13-14, 17, 27 and 30-31 stand rejected under 35 U.S.C. §

103(a) as being allegedly unpatentable over Durlam and Lee and further in view of Bronner et al. (U. S. Patent No. 6,242,770).

VIII. ARGUMENT

A. The Rejection of claims 11-12, 18, 26, 28, 33, 38-41 and 43 under 35 U.S.C. § 102(e) being allegedly anticipated by Lee et al. (U.S. Patent No. 5,895,947)

As set forth on pages 2-3 of the Office Action dated December 15, 2004, the Examiner rejected claims 11-12, 18, 26, 28, 33, 36, 38-41 and 43 under 35 U.S.C. § 102(e) over Lee, stating:

"Regarding claims 11-12, 18, 26, 28, 33, 38, 40 and 43, Lee (Fig. 8) discloses an Array of microelectronic elements comprising: a substrate 100 of semiconductor material (column 4, lines 54-56); a lower layer 110/120/130/134 of dielectric material disposed with a lower surface in contact with the substrate 100 and an upper surface in spaced adjacent thereto; a pattern of mutually electrically isolated conducting regions disposed within the lower layer 110/120/130/134 of dielectric material (column 5, lines 22-36), the conducting regions extending to the upper surface of the lower layer; an upper laver of dielectric material 30 (not shown in Fig. 8. see Fig. 1 and column 6, lines 10-18) disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer; and a plurality of capacitor nodes 142 made of polysilicon semiconductor material (column 5, lines 58-63) disposed within the upper layer of dielectric material 30 (also see Fig. 1), each of the nodes 142 being in electrical contact with only one of the conducting regions at the upper surface of the lower layer, wherein each conducting region comprises: a metal conductor (not labeled, see a first level interconnect wiring layer formed in a dielectric film 110 and column 2, lines 3-5); and a via e1 (not labeled in Fig. 8, see Fig. 6) which is filled with a TiN or W material (column 5, lines 22-30), the TiN or W material e1 extending between the metal conductor and a node 142 in the plurality of nodes and electrically connecting the metal conductor with the node 142 of capacitor semiconductor device. It is noted that the via filed with TiN or

W material of Lee would inherently function as diffusion barrier because it is filed with the same diffusion barrier material as claimed (i.e., TiN, W).

Regarding claim 36, Lee (Fig. 8) further discloses a bonding promoting layer 134 formed on the lower layer of dielectric material, the bonding promoting layer 134 bonding the lower surface of the upper layer 30 of dielectric material to the upper surface of the lower layer 110/120/130.

Regarding claims 39 and 41, Lee (Fig. 8) further discloses that the via e1 comprises an area which is less than an area of the metal conductor, and the node 142 which is electrically connected to the metal conductor is aligned with the via e1 and the metal conductor."

1. Independent claim 11

Independent claim 11 recites:

"An array of microelectronic elements comprising:

a substrate of semiconductor material;

a lower layer of dielectric material disposed with a lower surface in contact with said substrate and an upper surface in spaced adjacency thereto;

a pattern of mutually electrically isolated conducting regions disposed within said lower layer of dielectric material, said conducting regions extending to said upper surface of said lower layer;

an upper layer of dielectric material disposed with a lower surface thereof in contact with and bonded to said upper surface of said lower layer;

a plurality of nodes of semiconductor material disposed within said upper layer of dielectric material, each of said nodes being in electrical contact with only one of said conducting regions at said upper surface of said lower layer; and

a bonding promoting layer formed on said lower layer of dielectric material, said bonding promoting layer bonding said lower surface of said upper layer of dielectric material to said upper surface of said lower layer,

wherein each conducting region comprises:

a metal conductor; and

a via which is filled with a diffusion barrier material, said diffusion barrier material extending between said metal conductor and a node in said plurality of nodes and electrically connecting said metal conductor with said node." (emphasis added)

Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law.

Specifically, Appellant submits that there are elements of the claimed invention that are neither taught or suggested by Lee.

Lee discloses a process of fabricating a memory device which is intended to be simple and reduce a step height between the cell array region and the peripheral circuit region (Lee at col. 4, lines 12-16).

Contrary to the Examiner's allegations, Lee does not teach or suggest "*a bonding promoting layer formed on said lower layer of dielectric material, said bonding promoting layer bonding said lower surface of said upper layer of dielectric material to said upper surface of said lower layer*", as recited, for example, in claim 11 and similarly recited in claims 26 and 38.

As noted above, unlike conventional devices, the claimed invention forms, in a lower dielectric layer, a via on a metal conductor which is filled with a diffusion barrier material, and forms, in an upper dielectric layer, a plurality of nodes (e.g., Application at page 8, lines 3-16; Figure 5B). Further, a bonding promoting layer is formed on the lower dielectric layer, the bonding promoting layer bonding the upper dielectric layer to the lower dielectric layer (Application at page 13, lines 9-12).

In particular, the bonding promoting layer may help to promote bonding between the first dielectric layer and the second dielectric layer, when the inventive array is formed using a bonding process such as the SmartCutR process (Application at page 11, lines 1-18).

Clearly, Lee does not teach or suggest these novel features. Indeed, Lee **does not even disclose any bonding process but merely teaches depositing layer on top of layer, and so on** (e.g., see Figures 2-8 of Lee). Certainly, Lee does not teach or suggest a bonding promoting layer which bonds first and second dielectric layers.

Indeed, the Examiner attempts to equate the second capping layer 134 with the

bonding promoting layer of the claimed invention. However, this is completely unreasonable.

In fact, Lee teaches that the second capping layer is made of Si_3N_4 (Lee at col. 5, lines 8-10). Further, the capping layer 134 is formed between the oxide film 130 and the dielectric film 140. Importantly, nowhere does Lee teach or suggest that the layer 134 may include some form of "bonding promotion characteristic". In fact, Lee provides no support for the Examiner's statement that the layer 134 is a bonding promoting layer. Indeed, **the Examiner appears to have simply fabricated this characteristic out of thin air, on a whim, in a desperate attempt to support his allegations.**

Moreover, Appellant would point out that nowhere does Lee teach or suggest that layer 140 is bonded to layer 130. In fact, Lee only teaches that the layer 140 is "formed by forming an insulating film such as an oxide film on the entire surface of the resultant structure ... and removing the insulating film by etching the insulating film in the cell array region using the second capping layer 134 as an etch stop layer" (Lee at col. 5, lines 49-56). That is, Lee certainly does not teach that layer 140 is bonded to layer 130. Therefore, **clearly there is no need for a "bonding promoting layer" as unreasonably suggested by the Examiner.**

Further, Appellant would point out that by definition, a bonding promoting layer is a layer that promotes bonding. The term "promote" may be defined as "to contribute to the growth or prosperity of" (*Webster's Universal Encyclopedic Dictionary*, Barnes and Noble Books (2002), p. 1464). Appellant respectfully submits that the **layer 134 in Lee is not intended to promote and, in fact, does not promote the bonding of layers 130 and 140.** Indeed, there is no reason to suggest that the bond between layers 130 and 140 is any stronger because of layer 134, than if layer 134 was omitted entirely.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 11.

Therefore, the Board is respectfully requested to withdraw this rejection.

2. Independent Claim 26

Independent claim 26 recites:

"A microelectronic element array comprising:

a semiconductor substrate;

a first dielectric layer formed on said substrate;

a plurality of electrically isolated conductive regions disposed within said first dielectric layer, each conductive region comprising:

a metal conductor; and

a conductive via which is filled with a diffusion barrier material formed on said metal conductor;

a second dielectric layer having a lower surface which is bonded to an upper surface of said first dielectric layer;

a plurality of semiconductor nodes formed in said second dielectric layer, each semiconductor node contacting said conductive via and being electrically connected to said metal conductor by said conductive via; and

a bonding promoting layer formed on said first dielectric layer, said bonding promoting layer bonding said lower surface of said second dielectric layer to said upper surface of said first dielectric layer,

wherein said diffusion barrier material extends between said metal conductor and a node in said plurality of nodes."(emphasis added)

Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, Lee does not teach or suggest "*a bonding promoting layer formed on said first dielectric layer, said bonding promoting layer bonding said lower surface of said second dielectric layer to said upper surface of said first dielectric layer*" as recited in claim 26.

Appellant notes that these features are similar to the features discussed above with respect to claim 11. Therefore, Appellant's arguments made above with respect to claim 11 are incorporated by reference herein.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 26.

Therefore, the Board is respectfully requested to withdraw this rejection.

3. Independent claim 38

Independent claim 38 recites:

" A microelectronic element array comprising:

a first dielectric layer formed on a substrate;

at least one electrically isolated conductive region formed in said first dielectric layer, said at least one conductive region comprising:

a metal conductor; and

a conductive via which is filled with a diffusion barrier material formed on said metal conductor;

a second dielectric layer which is bonded to said first dielectric layer; and

at least one semiconductor node formed in said second dielectric layer, said at least one semiconductor node being formed on and contacting said at least one conductive region; and

a bonding promoting layer formed on said first dielectric layer, said bonding promoting layer bonding a lower surface of said second dielectric layer to an upper surface of said first dielectric layer,

wherein said diffusion barrier material extends between said metal conductor and said at least one semiconductor node and electrically connects said metal conductor to said at least one semiconductor node." (emphasis added)

Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, Lee does not teach or suggest "*a bonding promoting layer formed on said first dielectric layer, said bonding promoting layer bonding said lower surface of said second dielectric layer to said upper surface of said first dielectric layer*" as recited in claim 38.

Appellant notes that these features are similar to the features discussed above with respect to claim 11. Therefore, Appellant's arguments made above with respect to claim 11 are incorporated by reference herein.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 26.

Therefore, the Board is respectfully requested to withdraw this rejection.

4. Dependent Claim 12

Claim 12 depends from claim 11 and further recites *"wherein each of said nodes comprises a semiconductor device"*. This feature is discussed in the present Application at page 7, lines 8-10.

The Examiner asserts that this feature is disclosed in Lee at col. 5, lines 58-63.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 12. Therefore, the Board is respectfully requested to withdraw this rejection.

5. Dependent Claim 18

Claim 18 depends from claim 11 and further recites *"wherein said electrically conducting material comprises at least one of W, Ti, and Ta"*. This feature is discussed in the present Application at page 8, lines 3-7.

The Examiner asserts that this feature is disclosed in Lee at col. 5, lines 22-30.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 18. Therefore, the Board is respectfully requested to withdraw this rejection.

6. Dependent Claim 28

Claim 28 depends from claim 26 and further recites *"wherein each conductive region extends from said substrate to said upper surface of said first dielectric layer"*. This feature is discussed in the present Application at page 7, lines 3-7; Figure 5B.

The Examiner asserts that this feature is disclosed in Lee at col. 5, lines 22-30.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 28. Therefore, the Board is respectfully requested to withdraw this rejection.

7. Dependent Claim 33

Claim 33 depends from claim 26 and further recites *"wherein said via includes therein at least one of W, Ti, and Ta"*. This feature is discussed in the present Application at page 12, lines 1-5.

The Examiner asserts that this feature is disclosed in Lee at col. 5, lines 22-30.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 33. Therefore, the Board is respectfully requested to withdraw this rejection.

8. Dependent Claim 39

Claim 39 depends from claim 11 and further recites *"wherein said via comprises an area which is less than an area of said metal conductor"*. This feature is discussed in the present Application at page 8, lines 3-15; Figure 5B.

The Examiner asserts that this feature is disclosed in Lee at Figure 8.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 39. Therefore, the Board

is respectfully requested to withdraw this rejection.

9. Dependent Claim 40

Claim 40 depends from claim 11 and further recites *"wherein said diffusion barrier material comprises one of TiN, TaN and a TaSiN ternary alloy"*. This feature is discussed in the present Application at page 8, lines 3-15.

The Examiner asserts that this feature is disclosed in Lee at col. 5, lines 22-30.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 40. Therefore, the Board is respectfully requested to withdraw this rejection.

10. Dependent Claim 41

Claim 41 depends from claim 11 and further recites *"wherein said node which is electrically connected to said metal conductor is aligned with said via and said metal conductor"*. This feature is discussed in the present Application at Figure 5B.

The Examiner asserts that this feature is disclosed in Lee at Figure 8.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 41. Therefore, the Board is respectfully requested to withdraw this rejection.

11. Dependent Claim 43

Claim 43 depends from claim 11 and further recites *"wherein said metal conductor and said semiconductor material in said node are separated by said diffusion barrier material"*. This feature is discussed in the present Application at page 8, lines 3-15.

The Examiner does not specify where Lee allegedly discloses this feature.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 43. Therefore, the Board is respectfully requested to withdraw this rejection.

B. The rejection of claims 11-12, 15-16, 18, 26, 28-29, 33-35 and 36-38 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Durlam, et al. (U.S. Patent No. 5,940,319) and Lee

The Examiner rejected claims 11-12, 15-16, 18, 26, 28-29, 33-35, and 36-43 under 35 U.S.C. 103(a) as being unpatentable over Durlam et al (US. 5,940,319) in view of Lee et al (US. 5,895,947), stating:

"With respect to claims 11-12, 18, 26, 28-29, 33, 35, 38, and 40-43, Durlam's first embodiment (Figs. 5-8) discloses an array of microelectronic elements comprising: a substrate of semiconductor material 11; a lower layer of dielectric material (12a,21,25) disposed with a lower surface in contact with the substrate and an upper surface in spaced adjacency thereto; a pattern of mutually electrically isolated conducting regions (19a,37) and (19b,38) (Fig. 5) disposed within the lower layer of dielectric material, the conducting regions extending to the upper surface of the lower layer, an upper layer of dielectric material 51 disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer; and a plurality of nodes (43,45) and (44,46) comprising MTJs 43 and 44 and disposed within the upper layer of dielectric material, each of the nodes being in electrical contact with only one of the conducting regions at the upper surface of the lower layer, wherein each conducting region comprises: a metal conductor 19a and a via 37 formed on the metal conductor 19a, the via 37 extending between the metal conductor 19a and a node in the plurality of nodes and electrically connecting the metal conductor 19a with the node.

Durlam's first embodiment does not disclose the plurality of nodes including

semiconductor diodes. However, Durlam further teaches a second embodiment of ***MRAM*** *(Fig. 17) having a plurality of nodes, which include diodes 93 and 95 in contact with the conducting regions 82 at the upper surface of the lower layer. Accordingly, it would have been obvious to modify the first embodiment by forming the plurality of nodes with the structure as suggested by the second embodiment for the purpose of switching a magnetic memory element to read information in the magnetic memory element (column 6, lines 26-30).*

Neither Durlam's first embodiment nor Durlam's second embodiment discloses the via is filed with the refractory diffusion barrier material. However, Lee (Fig. 8) teaches the forming of a plurality of conducting regions, each conducting region comprises: a metal conductor and a via e1 (see Fig. 6) which is filled with a diffusion barrier material of TiN or W (column 5, lines 22-30), the diffusion barrier material e1 contacting capacitor semiconductor node 142 of polysilicon (column 5, lines 58-63) and extending between the metal conductor and the node 142. Accordingly, it would have been obvious to further modify Durlam's device by filling the via 37 with the refractory diffusion barrier material because as taught by Lee, such material would provide excellent filling properties (column 5, lines 25-27) and would reduce the contact resistance between the via and the semiconductor node (column 6, lines 33-41).

With respect to claim 16, Durlam (Fig. 8) further discloses that the device comprises a field effect transistor 12a, a first insulating layer 54 is disposed over an upper surface of the upper layer, and a second insulating layer 33 is formed over the upper surface of the lower layer.

Regarding claim 15, it would have been obvious to form the semiconductor node of Durlam as a field effect transistor because it is an intended use depending upon the application, which is desired for the semiconductor node of Durlam.

Regarding claim 34, Durlam (Fig. 8) also discloses that each of the conductive region further comprises a metal layer 31 (or 24) in electrical contact with the via, the metal layer 31 (or 24) being formed of nickel-iron (column 3, lines 28-30) which is different than the aluminum/copper material of the via 37.

Regarding claims 36-37, Durlam's Fig. 7 further discloses a bonding promoting

layer 33 of dielectric material formed on the lower layer 25 of dielectric material, the bonding promoting layer 33 bonding the lower surface of the upper layer 51 of dielectric material to the upper surface of the lower layer 33. As taught by Durlam, ***the bonding promoting layer 33 is placed between the lower layer 25 and the upper layer 51 to provide electrical isolation between the conductor layers (column 3, lines 60-64).*** *Therefore, it would have been obvious to form the dielectric layer 33 as a glass layer because the glass layer would also provide the electrical isolation between the conductor layers. It is noted that the process limitation (softening temperature in a range of 400 degrees C to 500 degrees c) would not carry patentable weight in a claim drawn to structure because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985). (emphasis added)*

Regarding claim 39, Lee (Fig. 8) also teaches the via e1 comprising an area which is less than an area of the metal conductor formed below.

1. Independent claim 11

Independent claim 11 recites:

"An array of microelectronic elements comprising:

a substrate of semiconductor material;

a lower layer of dielectric material disposed with a lower surface in contact with said substrate and an upper surface in spaced adjacency thereto;

a pattern of mutually electrically isolated conducting regions disposed within said lower layer of dielectric material, said conducting regions extending to said upper surface of said lower layer;

an upper layer of dielectric material disposed with a lower surface thereof in contact with and bonded to said upper surface of said lower layer;

a plurality of nodes of semiconductor material disposed within said upper layer of dielectric material, each of said nodes being in electrical contact with only one of said conducting regions at said upper surface of said lower layer; and

a bonding promoting layer formed on said lower layer of dielectric material, said bonding promoting layer bonding said lower surface of said upper layer of dielectric

material to said upper surface of said lower layer,

wherein each conducting region comprises:

a metal conductor; and

a via which is filled with a diffusion barrier material, said diffusion barrier material extending between said metal conductor and a node in said plurality of nodes and electrically connecting said metal conductor with said node." (emphasis added)

Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law.

Durlam discloses a magnetic random access memory (MRAM) which includes magnetic memory elements. A digit line and bit line are placed under and on top of the memory element. The lines are enclosed by a high permeability layer excluding a surface facing the memory element, which shields and focuses a magnetic field toward the memory element (Durlam at Abstract).

Appellant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters. Specifically, the Durlam device is merely intended to prevent a magnetic memory element from thermal degradation during fabrication (Durlam at col. 1, lines 61-64), whereas Lee is directed to a process which can reduce a step height between the cell array region and the peripheral circuit region (Lee at col. 4, lines 12-16). Clearly, no person of ordinary skill in the art would have considered combining these references.

Further, Appellant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, these references clearly do not teach or suggest their combination. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Durlam, nor Lee, nor any alleged combination thereof, teaches or suggests "*a bonding promoting layer formed on said lower layer of dielectric material, said bonding promoting layer bonding said lower surface of said upper layer of dielectric*

material to said upper surface of said lower layer", as recited, for example, in claim 11 and similarly recited in claims 26 and 38.

As noted above, unlike conventional devices, in the claimed invention, a bonding promoting layer is formed on the lower dielectric layer, the bonding promoting layer bonding the upper dielectric layer to the lower dielectric layer (Application at page 13, lines 9-12). The bonding promoting layer may help to promote bonding between the first dielectric layer and the second dielectric layer, when the inventive array is formed using a bonding process such as the SmartCutR process (Application at page 11, lines 1-18).

Clearly, Durlam does not teach or suggest these novel features. Indeed, the Examiner attempts to equate the dielectric layer 33 with the bonding promoting layer of the claimed invention. However, this is clearly unreasonable.

Indeed, the Examiner recognizes in the Office Action that the dielectric layer 33 "is placed between the lower layer 25 and the upper layer 51 **to provide electrical isolation between the conductor layers**" (emphasis added). The Examiner goes on to state that since the bonding promoting layer in the claimed invention can include glass, and since glass may provide electrical isolation, that it "would have been obvious to form the dielectric layer 33 as a glass layer because the glass layer would also provide the electrical isolation between the conductor layers" (Office Action at page 6). Appellant respectfully submits that **the Examiner's argument here is completely unreasonable**.

Indeed, Appellant would point out that the Examiner does not even attempt to allege that the layer 33 is intended to have any type of "bonding promoting" characteristic. Indeed, the layer 33, as the Examiner correctly points out, is merely intended to provide electrical isolation. In fact, nowhere does Durlam teach or suggest that conductor layer 34 is "bonded to" the digit lines 29 and 30, but merely states that the layer 34 is "deposited". Thus, there is no need for a "bonding promoting layer" in Durlam.

Moreover, the Examiner attempts to rely on Figure 17 in Durlam to support his position that Durlam teaches a plurality of nodes of semiconductor material. However, the Examiner's reliance on Figure 17 in Durlam is completely unreasonable.

In fact, the Application expressly states that claimed invention may be used to overcome a problem in conventional devices such as that shown in Figure 17 of Durlam.

Namely, the claimed invention can help to avoid a reaction between **the metal conductor and the semiconductor node (when the conductor and node are in direct contact) which can make devices unreliable** (Application at page 8, lines 3-15).

Specifically, the claimed invention, includes a via formed on the metal conductor and filled with a diffusion barrier material which extends between the metal conductor and a semiconductor node and electrically connects the metal conductor with the semiconductor node. (Application at page 8, lines 3-16; Figure 5B). The diffusion barrier material keeps a metal conductor (e.g., word line) from reacting with the semiconductor material (e.g., silicon diode). Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum for improved performance (Application at page 8, lines 3-16).

Clearly, Durlam does not teach or suggest this feature. Indeed, Durlam does not even discuss at least one of the problems (e.g., reaction between a semiconductor node and a metal conductor (e.g., a word line)) which the claimed invention was intended to address.

The Examiner also attempts to rely on Figures 5-8 in Durlam to support his allegations. Specifically, the Examiner attempts to equate the metal conductor 37 in Durlam with the via in the conducting region of the claimed invention (e.g., via 13 in the exemplary embodiment illustrated in Figures 5A-5B of the Application). However, the Examiner is completely incorrect.

In particular, the Examiner relies on col. 3, lines 35-42 to support his allegation that the via includes Ta (e.g., a diffusion barrier material). However, this passage merely refers to Figure 3, stating:

> "In order to improve adhesion of field focusing layer 24 and to provide a barrier for Ni or Fe diffusion into the conductor and/or dielectric a layer of Ta or TaN or such materials could be added **between field focusing layer 24 and conductor layer 26**" (Durlam at col. 3, lines 39-42) (emphasis added). Appellant notes that conductor layer 26 eventually becomes the metal conductor 37 illustrated in Figure 5 in Durlam. Therefore, Durlam merely teaches that a "barrier" may be provided **before forming the metal conductor** 37. That is, nowhere does this passage or Figure 3 in Durlam teach or suggest that the metal conductor 37 includes barrier material.

It is **also important to note that Durlam teaches that the conductor line 45 (which the Examiner attempts to equate with the node in the claimed invention)** directly contacts the conductor 37. That is, even assuming that a refractory metal layer is formed beneath the conductor 37, the conductor line 45 still contacts mostly the conductor 37 which does not include any refractory metal. Thus, this embodiment of Durlam clearly does not teach or suggest the importance of separating a node from an aluminum/copper conductor in order to avoid any interaction between the a node and an aluminum/copper conductor.

Moreover, even if is it assumed (arguendo) that the metal conductor 37 includes a diffusion barrier material, the metal conductor 37 still cannot reasonably be equated with the via of the claimed invention. Indeed, in the claimed invention, the via extends between the metal conductor and a semiconductor node and electrically connects the metal conductor with the semiconductor node. (Application at page 8, lines 3-16; Figure 5B). In fact, the via in the claimed invention may be used to prevent the metal conductor from reacting with a semiconductor node, such as a silicon diode.

Durlam, on the other hand, teaches that the metal conductor 37 is used to "electrically connect plug conductors 19a and 19b to conductor layer 34" (Durlam at col. 3, line 67). That is, the metal conductor 37 electrically connects the plug conductors 19a, 19b to the metal conductor layer 45, as illustrated in Figure 7 (e.g., see Durlam at Abstract). Therefore, **the function of the metal conductor 37 is completely different that the function of the via in the claimed invention.**

For example, in the exemplary embodiment illustrated in Figure 5A, the via includes a diffusion barrier material which extends between the word line 15 and a diode mesa including Si layer 3'. Thus, the via may be used to electrically connect the metal conductor with the semiconductor node.

In fact, the Examiner expressly concedes that the portion of Durlam on which he is relying as disclosing the claimed invention, does not teach or suggest this feature. However, the Examiner **refers to the embodiment of Figure 17 (e.g., a completely unrelated aspect) in Durlam** as allegedly disclosing this feature. That is, Figure 17 in Durlam is completely unrelated to the embodiment in Figure 5 of Durlam.

Moreover, Figure 17 in Durlam teaches forming a semiconductor diode in direct

contact with an aluminum/copper conductor. Appellant would respectfully point out that the Application expressly teaches that such a device is not reliable. Indeed, that is one of the problems which the claimed invention is intended to solve.

Appellant would respectfully submit that it is absolutely unreasonable for the Examiner to attempt to rely on Figure 17 in Durlam as somehow teaching the claimed invention, when Figure 17 expressly teaches one of the very problems (e.g., reaction between an Al/Cu layer and a semiconductor) which the claimed invention was intended to solve.

Indeed, an important point for the Examiner to consider is that Durlam clearly does not teach or suggest the importance of forming a diffusion barrier between a metal conductor an a semiconductor node, which is an important feature of the claimed invention. Indeed, Durlam specifically teaches that it is desirable to form a semiconductor directly in contact with the metal conductor. That is, Durlam teaches away from the claimed invention.

Further, Appellant would respectfully submit that the Examiner **must read the Durlam reference as a whole.** He can not merely search throughout the reference willy-nilly, and picking and choosing unrelated features to somehow kluge together a basis for his unreasonable rejection. In this instance, the Examiner is relying on alleged features from completely unrelated and different aspects to support his position, which cannot form the basis for his rejection. Clearly, the embodiment of Figure 17 would not have been combined with the unrelated embodiment of Figure 5, and the Examiner has failed to provide any adequate motivation or suggestion for such combination.

Moreover, even assuming that the embodiment of Figure 17 would have been combined with the embodiment of Figure 5, the alleged combination would not teach or suggest a conductive via which includes a via formed on the metal conductor and filled with a diffusion barrier material which extends between the metal conductor and a semiconductor node and electrically connects the metal conductor with the semiconductor node.

Indeed, Figure 17 does not even teach or suggest a "via" as in the claimed invention, but instead illustrates **a diode 95 formed directly on a metal conductor 82.** Certainly, Figure 17 does not teach or suggest a via which is filled with a diffusion barrier material

extending between a metal conductor and a semiconductor node.

Therefore, contrary to the Examiner's allegations, nowhere does Durlam teach or suggest the conductive via of the claimed invention.

Therefore, Appellant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

Therefore, the Board is respectfully requested to withdraw this rejection.

2. Independent Claim 26

Independent claim 26 recites:

"A microelectronic element array comprising:

a semiconductor substrate;

a first dielectric layer formed on said substrate;

a plurality of electrically isolated conductive regions disposed within said first dielectric layer, each conductive region comprising:

a metal conductor; and

a conductive via which is filled with a diffusion barrier material formed on said metal conductor;

a second dielectric layer having a lower surface which is bonded to an upper surface of said first dielectric layer;

a plurality of semiconductor nodes formed in said second dielectric layer, each semiconductor node contacting said conductive via and being electrically connected to said metal conductor by said conductive via; and

a bonding promoting layer formed on said first dielectric layer, said bonding promoting layer bonding said lower surface of said second dielectric layer to said upper surface of said first dielectric layer,

wherein said diffusion barrier material extends between said metal conductor and a node in said plurality of nodes."(emphasis added)

Appellant respectfully submits that the Examiner's position is flawed as a matter of

fact and as a matter of law.

Specifically, neither Durlam, nor Lee nor any alleged combination teaches or suggests "*a bonding promoting layer formed on said first dielectric layer, said bonding promoting layer bonding said lower surface of said second dielectric layer to said upper surface of said first dielectric layer*" as recited in claim 26.

Appellant notes that these features are similar to the features discussed above with respect to claim 11. Therefore, Appellant's arguments made above with respect to claim 11 are incorporated by reference herein.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 26.

Therefore, the Board is respectfully requested to withdraw this rejection.

3. Independent claim 38

Independent claim 38 recites:

" A microelectronic element array comprising:

a first dielectric layer formed on a substrate;

at least one electrically isolated conductive region formed in said first dielectric layer, said at least one conductive region comprising:

a metal conductor; and

a conductive via which is filled with a diffusion barrier material formed on said metal conductor;

a second dielectric layer which is bonded to said first dielectric layer; and

at least one semiconductor node formed in said second dielectric layer, said at least one semiconductor node being formed on and contacting said at least one conductive region; and

a bonding promoting layer formed on said first dielectric layer, said bonding promoting layer bonding a lower surface of said second dielectric layer to an upper surface of said first dielectric layer,

wherein said diffusion barrier material extends between said metal conductor and said at least one semiconductor node and electrically connects said metal conductor to said

at least one semiconductor node." (emphasis added)

Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law.

Specifically, neither Durlam, nor Lee nor any alleged combination teaches or suggests "*a retrieval unit for retrieving the caller's profile to construct a personalized IVR dialogue menu by performing a tree-based collapsing and play-out the personalized menu*" or a personalized menu which includes *"a plurality of shortcut paths; and an option for changing said plurality of shortcut paths in said personalized IVR dialogue menu*" as recited in claim 38.

Appellant notes that these features are similar to the features discussed above with respect to claim 11. Therefore, Appellant's arguments made above with respect to claim 11 are incorporated by reference herein.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 38.

Therefore, the Board is respectfully requested to withdraw this rejection.

4. Dependent Claim 12

Claim 12 depends from claim 11 and further recites *"wherein each of said nodes comprises a semiconductor device"*. This feature is discussed in the present Application at page 7, lines 8-10.

The Examiner asserts that this feature is disclosed in Durlam at Figure 17.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that neither Durlam, nor Lee nor any alleged combination thereof teaches or suggests each and every element of the claimed invention as recited in claim 12. Therefore, the Board is respectfully requested to withdraw this rejection.

5. Dependent Claim 15

Claim 15 depends from claim 12 and further recites *" wherein said semiconductor device comprises a field effect transistor"*. This feature is discussed in the present Application at page 7, lines 8-10.

The Examiner concedes that this feature is not taught or suggested by the cited references but alleges that "it would have been obvious to form the semiconductor node of Durlam as a field effect transistor because it is an intended use depending upon the application".

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that neither Durlam, nor Lee nor any alleged combination thereof teaches or suggests each and every element of the claimed invention as recited in claim 15. Therefore, the Board is respectfully requested to withdraw this rejection.

6. Dependent Claim 16

Claim 16 depends from claim 15 and further recites *"wherein a first insulating layer is disposed over an upper surface of said upper layer and a second insulating layer is formed over said upper surface of said lower layer"*. This feature is discussed in the present Application at page 7, lines 13-16.

The Examiner asserts that this feature is disclosed in Durlam at Figure 8.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that neither Durlam, nor Lee nor any alleged combination thereof teaches or suggests each and every element of the claimed invention as recited in claim 16. Therefore, the Board is respectfully requested to withdraw this rejection.

7. Dependent Claim 18

Claim 18 depends from claim 11 and further recites *"wherein said electrically conducting material comprises at least one of W, Ti, and Ta"*. This feature is discussed in the present Application at page 8, lines 3-7.

The Examiner asserts that this feature is disclosed in Lee at col. 5, lines 22-30.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that neither Durlam, nor Lee nor any alleged combination thereof teaches or suggests each and every element of the claimed invention as recited in claim 18. Therefore, the Board is respectfully requested to withdraw this rejection.

8. Dependent Claim 28

Claim 28 depends from claim 26 and further recites *" wherein each conductive region extends from said substrate to said upper surface of said first dielectric layer"*. This feature is discussed in the present Application at page 9, lines 8-18.

The Examiner asserts that this feature is disclosed in Lee at col. 5, lines 58-63.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that neither Durlam, nor Lee nor any alleged combination thereof teaches or suggests each and every element of the claimed invention as recited in claim 28. Therefore, the Board is respectfully requested to withdraw this rejection.

9. Dependent Claim 29

Claim 29 depends from claim 26 and further recites *"wherein each conductive region further comprises a word line, said via being formed on said word line"*. This feature is discussed in the present Application at page 8, lines 3-15.

The Examiner does not expressly state where this feature is taught or suggested by the cited references.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that neither Durlam, nor Lee nor any alleged combination thereof teaches or suggests each and every element of the claimed invention as recited in claim 29. Therefore, the Board is respectfully requested to withdraw this rejection.

10. Dependent Claim 33

Claim 33 depends from claim 26 and further recites *"wherein said via includes therein at least one of W, Ti, and Ta"*. This feature is discussed in the present Application at page 8, lines 3-15.

The Examiner asserts that this feature is disclosed in Lee at col. 5, lines 22-30.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that neither Durlam, nor Lee nor any alleged combination thereof teaches or suggests each and every element of the claimed invention as recited in claim 33. Therefore, the Board is respectfully requested to withdraw this rejection.

11. Dependent Claim 34

Claim 34 depends from claim 26 and further recites *"wherein each said conductive region further comprises a metal layer in electrical contact with said via, said metal layer being formed of a different material than said via"*. This feature is discussed in the present Application at page 8, lines 3-15.

The Examiner asserts that this feature is disclosed in Durlam at Figure 8 and col. 3, lines 28-30.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that neither Durlam, nor Lee nor any alleged combination thereof teaches or suggests each and every element of the claimed invention as recited in claim 34. Therefore, the Board is respectfully requested to withdraw this rejection.

12. Dependent Claim 35

Claim 35 depends from claim 29 and further recites *"wherein said via includes therein a refractory metal and said word line comprises one of copper and aluminum"*. This feature is discussed in the present Application at page 8, lines 3-15.

The Examiner asserts that this feature is disclosed in Durlam at col. 3, lines 28-30.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that neither Durlam, nor Lee nor any alleged combination thereof teaches or suggests each and every element of the claimed invention as recited in claim 35. Therefore, the Board is respectfully requested to withdraw this rejection.

13. Dependent Claim 37

Claim 37 depends from claim 1 and further recites *"wherein said bonding promoting layer comprises a glass layer having a softening temperature in a range of 400°C to 500°C"*. This feature is discussed in the present Application at page 13, lines 9-12.

The Examiner asserts that this feature is disclosed in Durlam at col. 3, lines 60-64.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that neither Durlam, nor Lee nor any

alleged combination thereof teaches or suggests each and every element of the claimed invention as recited in claim 37. Therefore, the Board is respectfully requested to withdraw this rejection.

C. The Rejection of claims 13-14, 17, 27 and 30-31 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Durlam and Lee and further in view of Bronner et al. (U. S. Patent No. 6,242,770)

The Examiner rejects claims 13-14, 17, 27, and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al and Lee et al as applied to claims 11 and 26 above, and further in view of Bronner et al (US. 6,242,770), stating:

"Durlam does not disclose that diodes are single crystal Si diodes.

However, it would have been obvious to form Durlam's diodes as single crystal Si diodes because according to Bronner, such single crystal Si diodes (column 9, lines 63-65) would provide high conductivity, high rectification and low total resistance (column 3, lines 1-4)."

In addition, the Examiner responded to Appellant's arguments in the Amendment filed on September 30, 2004, stating:

"In the amendment filed 9/30/04, the scopes of base claims are changed and narrower by deleting "comprising" and inserting "which is filled with". Therefore, the new ground of rejection is applied.

Applicant argues that "Durlam clearly does not teach or suggest the importance of forming a diffusion barrier between a metal conductor and a semiconductor node," as amended.

This argument is not persuasive because the new reference issued to Lee et al (US. 5,895,947) clearly teaches the obviousness of forming a conducting region comprising: a via el filled with a diffusion barrier material and disposed between a metal conductor and a semiconductor node 142 of polysilicon (see Fig. 8). The via filled with the diffusion barrier material would provide excellent filling properties (column 5, lines 25-27) and reducing the contact resistance between the via and the semiconductor

node (column 6, lines 33-41).

Applicant asserts that Applicant surprises because the examiner relies on the teaching disclosed in figure 5 and the teaching disclosed in figure 17 of Durlam for the combination. According to Applicant, the embodiment "disclosed in Figure 17 of Durlam which is completely unrelated to the embodiment in Figure 5 of Durlam."

The examiner recognizes that one skilled in the art would not be surprised by the combination between these two embodiments because they are completely related to magnetic random access memory structure (MRAM), and because the motivation for the combination of these embodiments is clearly suggested (see ground of rejection for details).

Applicant also argues that it would not be obvious to combine Bronner with the applied references because Bronner does not teach or suggest a via formed on the metal conductor, and filled with a diffusion barrier as amended.

This argument is not persuasive because the new reference issued to Lee et al clearly suggests a via formed on the metal conductor and filled with a diffusion barrier material. Bronner is only relied on for showing that it was known to form a diode as a single crystal Si diode for providing high conductivity, high rectification and low total resistance (column 3, lines 1-4).

1. Dependent Claim 13

Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law.

Appellant respectfully submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Bronner discloses a magneto-resistive memory cell which includes a substrate, monocrystalline diode formed in the substrate, a first conductor in the substrate and a second conductor formed above a magnetic tunnel junction formed on the diode (Bronner at Abstract).

Appellant submits that Durlam, Lee and Bronner are directed to different matters and, therefore, would not have been combined as alleged by the Examiner. Indeed, the Durlam

device is merely intended to prevent a magnetic memory element from thermal degradation during fabrication (Durlam at col. 1, lines 61-64), Lee is directed to a process of fabricating a memory cell which can reduce a step height between the cell array region and the peripheral circuit region (Lee at col. 4, lines 12-16), whereas Bronner is intended to minimize the resistance of a diode in a memory cell (Bronner at col. 3, lines 3-4). Clearly, no person of ordinary skill in the art would have considered combining these references.

Further, Appellant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that "[i]t would have been obvious to form Durlam's diodes as single crystal Si diodes because according to Bronner, such single crystal Si diodes ... would provide high conductivity, high rectification, and low total resistance" which is insufficient to support the combination.

Moreover, neither Durlam, nor Lee, nor Bronner, nor any alleged combination thereof, teaches or suggests "*a bonding promoting layer formed on said lower layer of dielectric material, said bonding promoting layer bonding said lower surface of said upper layer of dielectric material to said upper surface of said lower layer*", as recited, for example, in claim 11 and similarly recited in claims 26 and 38.

Clearly, Bronner does not teach or suggest these novel features. Indeed, the Examiner merely relies on Bronner as allegedly teaching another feature of the claimed invention and does not allege that Bronner teaches or suggests this feature.

Further, Bronner merely discloses a diode 514 which is in the shape of a V-groove formed in an insulation layer 100. A metal conductor 525 is formed on the diode 514 and an oxide layer 530 is formed on the metal conductor 525 (Bronner at Figure 5B). This structure is completely unrelated to the claimed invention.

In fact, like Lee and Durlam, nowhere does Bronner teach or suggested a second dielectric layer bonded to a first dielectric layer. Therefore, Bronner certainly does not teach or suggest a bonding promoting layer. Thus, Bronner clearly does not make up for the deficiencies of Durlam and Lee.

Therefore, Appellant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the

claimed invention

In addition, claim 13 depends from claim 11 and further recites *"wherein said semiconductor material comprises oriented single crystal grain, monocrystalline semiconductor material, and each of said nodes comprises a diode"*. This feature is discussed in the present Application at page 7, lines 3-10.

The Examiner alleges that Bronner teaches this feature at col. 3, lines 1-4.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 13. Therefore, the Board is respectfully requested to withdraw this rejection.

2. Dependent Claim 14

Claim 14 depends from claim 13 and further recites *"wherein said microelectronic elements comprise magnetoresistive memory elements each comprising a said diode and an MTJ structure"*. This feature is discussed in the present Application at page 7, lines 8-10.

The Examiner does not clearly specify where the cited references teach or suggest this feature.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 14. Therefore, the Board is respectfully requested to withdraw this rejection.

3. Dependent Claim 17

Claim 17 depends from claim 13 and further recites *"wherein said oriented single crystal grain semiconductor material is oriented in the <100> orientation"*. This feature is discussed in the present Application at page 7, lines 3-7.

The Examiner does not clearly specify where the cited references teach or suggest this feature.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 17. Therefore, the Board is respectfully requested to withdraw this rejection.

4. Dependent Claim 27

Claim 27 depends from claim 26 and further recites *"wherein said plurality of semiconductor nodes comprises a plurality of monocrystalline semiconductor diodes"*. This feature is discussed in the present Application at page 7, lines 3-7.

The Examiner does not clearly specify where the cited references teach or suggest this feature.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 27. Therefore, the Board is respectfully requested to withdraw this rejection.

5. Dependent Claim 30

Claim 30 depends from claim 27 and further recites *"further comprising: a plurality of magnetic tunnel junction (MTJ) elements, each MTJ element in electrical contact with a diode in said plurality of monocrystalline semiconductor diodes"*. This feature is discussed in the present Application at page 9, lines 11-17.

The Examiner does not clearly specify where the cited references teach or suggest this feature.

However, Appellant respectfully submits that the Examiner's position is flawed as a

matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 30. Therefore, the Board is respectfully requested to withdraw this rejection.

5. Dependent Claim 31

Claim 31 depends from claim 30 and further recites *"wherein each said MTJ element and each said diode combine to form a memory element"*. This feature is discussed in the present Application at page 9, lines 11-17.

The Examiner does not clearly specify where the cited references teach or suggest this feature.

However, Appellant respectfully submits that the Examiner's position is flawed as a matter of fact and as a matter of law. Specifically, nowhere does the cited passage teach or suggest this feature.

Therefore, Appellant respectfully submits that Lee clearly does not teach or suggest each and every element of the claimed invention as recited in claim 31. Therefore, the Board is respectfully requested to withdraw this rejection.

Therefore, in short, the dependent claims of the present Application define elements and limitations which further place the claimed invention squarely in the realm of statutory subject matter and which provide a useful, tangible and concrete result.

Therefore, dependent claims like independent claims 11, 26 and 38, include at least one element which is not taught or suggested by the cited references, or any combination of the cited references.

In view of all of the foregoing, Appellant respectfully submits that the Examiner's rejections are erroneous as a matter of fact and law

VIII. CONCLUSION

In view of the foregoing, Appellant submits that claims 11-18, 26-31, 33-35 and 37-

43, all the claims presently pending in the application, are patentably distinct from the prior art of record and in condition for allowance. Thus, the Board is respectfully requested to remove the rejections of claims 11-18, 26-31, 33-35 and 37-43.

Please charge any deficiencies and/or credit any overpayments necessary to enter this paper to Assignee's Deposit Account number 50-0510.

Respectfully submitted,

Dated: 5/16/05

Phillip E. Miller
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CLAIMS APPENDIX

11. An array of microelectronic elements comprising:

a substrate of semiconductor material;

a lower layer of dielectric material disposed with a lower surface in contact with said substrate and an upper surface in spaced adjacency thereto;

a pattern of mutually electrically isolated conducting regions disposed within said lower layer of dielectric material, said conducting regions extending to said upper surface of said lower layer;

an upper layer of dielectric material disposed with a lower surface thereof in contact with and bonded to said upper surface of said lower layer;

a plurality of nodes of semiconductor material disposed within said upper layer of dielectric material, each of said nodes being in electrical contact with only one of said conducting regions at said upper surface of said lower layer; and

a bonding promoting layer formed on said lower layer of dielectric material, said bonding promoting layer bonding said lower surface of said upper layer of dielectric material to said upper surface of said lower layer,

wherein each conducting region comprises:

a metal conductor; and

a via which is filled with a diffusion barrier material, said diffusion barrier material extending between said metal conductor and a node in said plurality of nodes and electrically connecting said metal conductor with said node.

12. An array as set forth in claim 11, wherein each of said nodes comprises a semiconductor device.

13. An array as set forth in claim 11, wherein said semiconductor material comprises oriented single crystal grain, monocrystalline semiconductor material, and each of said nodes comprises a diode.

14. An array as set forth in claim 13, wherein said microelectronic elements comprise magnetoresistive memory elements each comprising a said diode and an MTJ structure.

15. An array as set forth in claim 12, wherein said semiconductor device comprises a field effect transistor.

16. An array as set forth in claim 15, wherein a first insulating layer is disposed over an upper surface of said upper layer and a second insulating layer is formed over said upper surface of said lower layer.

17. An array as set forth in claim 13, wherein said oriented single crystal grain semiconductor material is oriented in the <100> orientation.

18. An array as set forth in claim 11, wherein said electrically conducting material comprises at least one of W, Ti, and Ta.

26. A microelectronic element array comprising:

a semiconductor substrate;

a first dielectric layer formed on said substrate;

a plurality of electrically isolated conductive regions disposed within said first dielectric layer, each conductive region comprising:

a metal conductor; and

a conductive via which is filled with a diffusion barrier material formed on said metal conductor;

a second dielectric layer having a lower surface which is bonded to an upper surface of said first dielectric layer;

a plurality of semiconductor nodes formed in said second dielectric layer, each semiconductor node contacting said conductive via and being electrically connected to said metal conductor by said conductive via; and

a bonding promoting layer formed on said first dielectric layer, said bonding

promoting layer bonding said lower surface of said second dielectric layer to said upper surface of said first dielectric layer,

wherein said diffusion barrier material extends between said metal conductor and a node in said plurality of nodes.

27. The array according to claim 26, wherein said plurality of semiconductor nodes comprises a plurality of monocrystalline semiconductor diodes.

28. The array according to claim 26, wherein each conductive region extends from said substrate to said upper surface of said first dielectric layer.

29. The array according to claim 26, wherein each conductive region further comprises a word line, said via being formed on said word line.

30. The array according to claim 27, further comprising:

a plurality of magnetic tunnel junction (MTJ) elements, each MTJ element in electrical contact with a diode in said plurality of monocrystalline semiconductor diodes.

31. The array according to claim 30, wherein each said MTJ element and each said diode combine to form a memory element.

33. The array according to claim 26, wherein said via includes therein at least one of W, Ti, and Ta.

34. The array according to claim 26, wherein each said conductive region further comprises a metal layer in electrical contact with said via, said metal layer being formed of a different material than said via.

35. The array according to claim 29, wherein said via includes therein a refractory metal and said word line comprises one of copper and aluminum.

37. The array as set forth in claim 11, wherein said bonding promoting layer comprises a glass layer having a softening temperature in a range of 400°C to 500°C.

38. A microelectronic element array comprising:

a first dielectric layer formed on a substrate;

at least one electrically isolated conductive region formed in said first dielectric layer, said at least one conductive region comprising:

a metal conductor; and

a conductive via which is filled with a diffusion barrier material formed on said metal conductor;

a second dielectric layer which is bonded to said first dielectric layer; and

at least one semiconductor node formed in said second dielectric layer, said at least one semiconductor node being formed on and contacting said at least one conductive region; and

a bonding promoting layer formed on said first dielectric layer, said bonding promoting layer bonding a lower surface of said second dielectric layer to an upper surface of said first dielectric layer,

wherein said diffusion barrier material extends between said metal conductor and said at least one semiconductor node and electrically connects said metal conductor to said at least one semiconductor node.

39. The array as set forth in claim 11, wherein said via comprises an area which is less than an area of said metal conductor.

40. The array as set forth in claim 11, wherein said diffusion barrier material comprises one of TiN, TaN and a TaSiN ternary alloy.

41. The array as set forth in claim 11, wherein said node which is electrically connected to said metal conductor is aligned with said via and said metal conductor.

42. The array as set forth in claim 11, wherein said node comprises a semiconductor diode.

43. The array as set forth in claim 11, wherein said metal conductor and said semiconductor material in said node are separated by said diffusion barrier material.

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Appeal Brief was filed by facsimile with the United States Patent and Trademark Office, Examiner Phat X Cao , Group Art Unit # 2814 at fax number (703) 872-9306 this 16th day of May, 2005.

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